Amendments to the Claims:

1. (Currently amended) A method of ~~operating~~ reducing noise voltage in a memory circuit, comprising the steps of:

activating a first signal line adjacent a control terminal of a memory cell;

coupling a voltage from the signal line to the control terminal of the memory cell;

applying a second control signal to the memory cell;

coupling the noise voltage to the memory cell in response to the step of applying the second control signal;

activating a precharge signal applied to a precharge circuit to precharge a bitline connected to the memory cell to a predetermined voltage;

activating a first control signal from an inactive state after the step of coupling while the precharge signal is active, the first control signal applied to ~~a~~ the control terminal of ~~a~~ the memory cell ~~transistor~~, the memory cell ~~transistor~~ having a current path connected to the bitline, wherein the noise voltage is conducted to the bitline through the current path; and

inactivating the precharge signal while the first control signal is active.

2. (Original) A method as in claim 1, wherein the memory cell comprises Lead Zirconate Titanate (PZT).

3. (Original) A method as in claim 1, wherein the memory cell comprises Strontium Bismuth Titanate (SBT).

4. (Original) A method as in claim 1, comprising the step of inactivating the first control signal while the precharge signal is active.

5. (Currently amended) A method as in claim 1, comprising the step of activating from an inactive state ~~a~~ the second control signal applied to the memory cell after the step of inactivating the precharge signal.

6. (Original) A method as in claim 5, comprising the steps of:

inactivating the second control signal while the first control signal is active; and

activating the precharge signal while the first control signal is active and the second control signal is inactive.

7. (Original) A method as in claim 6, wherein the first control signal is a wordline signal, and wherein the second control signal is a plateline signal.

8. (Original) A method as in claim 7, wherein the wordline signal is applied to a first wordline and not applied to a second wordline, and wherein the plateline signal is applied to memory cells connected to the first and the second wordline.

9. (Original) A method as in claim 1, wherein the step of activating a precharge signal precharges the bitline and a complementary bitline to the predetermined voltage.

10. (Original) A method as in claim 9, wherein the predetermined voltage is Vss.

Claims 11-17 (Canceled)

18. (Currently amended) A memory circuit, comprising:

a memory array arranged in rows and columns of memory cells, each row of memory cells connected to a respective wordline, each column of memory cells connected to one of a bitline and a complementary bitline, wherein an active wordline accesses a respective row of memory cells;

a plurality of precharge circuits, each precharge circuit connected to a respective column of memory cells and coupled to receive a precharge signal, wherein an active precharge signal renders a respective precharge circuit conductive; ~~and~~

a control circuit arranged to produce an active wordline signal from an inactive wordline signal while the precharge signal is active;

a plateline circuit arranged to apply a first plateline signal pulse to the respective row of memory cells to produce a difference voltage between the bitline and the complementary bitline and to apply a second plateline signal pulse to restore data to the respective row of memory cells; and

a sense amplifier circuit arranged to amplify the difference voltage.

19. (Original) A memory circuit as in claim 18, wherein the memory cells are ferroelectric memory cells.

20. (Cancel)

21. (Cancel)

22. (Original) A memory circuit as in claim 18, wherein each precharge circuit comprises:

a first transistor connected between a respective bitline and a voltage terminal;

a second transistor connected between a respective complementary bitline and the voltage terminal.

23. (Original) A memory circuit as in claim 22, wherein each precharge circuit comprises a third transistor connected between the respective bitline and the respective complementary bitline.

24. (Original) A memory circuit as in claim 22, wherein each column of memory cells is coupled to a respective sense amplifier, each sense amplifier arranged to amplify a difference voltage between one of a bitline or complementary bitline voltage and a reference voltage.

25. (Original) A memory circuit as in claim 24, wherein the reference voltage is applied to the other of the bitline or complementary bitline.

26. (Currently amended) A memory circuit, comprising:

a bitline;

a complementary bitline;

a voltage terminal;

a first access transistor connected to the bitline, the first access transistor having a first control terminal coupled to receive a first control signal arranged to turn the access transistor on;

a second access transistor connected to the complementary bitline, the second access transistor having a second control terminal coupled to receive the first control signal arranged to turn the second access transistor on;

a first precharge transistor having a current path coupled between the bitline and the voltage terminal, the first precharge transistor having a gate coupled to receive a precharge signal, wherein the precharge signal turns the first precharge transistor off and on while the first access transistor is on; ~~and~~

a second precharge transistor having a current path coupled between the complementary bitline and the voltage terminal, the second precharge transistor having a gate coupled to receive the precharge signal;

<u>a plateline circuit arranged to apply a first plateline signal pulse to a memory cell including the first and second access transistors to produce a difference voltage between the bitline and the complementary bitline and to apply a second plateline signal pulse to restore data to the memory cell; and</u>

<u>a sense amplifier circuit arranged to amplify the difference voltage</u>.

27. (Original) A memory circuit as in claim 26, wherein the memory circuit is a ferroelectric memory circuit.

28. (Original) A memory circuit as in claim 26, wherein each of the first and second control terminals is a wordline terminal.

29. (Currently amended) A memory circuit as in claim 26, comprising:

a third control terminal coupled to receive ~~a second control signal~~ the first and second plateline signal pulses; and

a first ferroelectric capacitor coupled between the first access transistor and the third control terminal; and

a second ferroelectric capacitor coupled between the second access transistor and the third control terminal.

30. (Currently amended) A memory circuit as in claim 29, wherein the ~~second control signal~~ first plateline signal pulse produces a voltage on the bitline and the complementary bitline after the precharge signal turns off the first and second precharge transistors.

31. (Original) A memory circuit as in claim 26, comprising a third precharge transistor having a current path coupled between the bitline and the complementary bitline, the third precharge transistor having a gate coupled to receive the precharge signal.

32. (Currently amended) A memory circuit, comprising:

a bitline;

a complementary bitline;

a voltage terminal;

an access transistor connected to the bitline, the transistor having a first control terminal coupled to receive a first control signal arranged to turn the access transistor on; ~~and~~

a first precharge transistor having a current path coupled between the bitline and the voltage terminal, the first precharge transistor having a gate coupled to receive a precharge signal, wherein the precharge signal turns the first precharge transistor off from an on state while the access transistor is on;

a plateline circuit arranged to apply a first plateline signal pulse to a memory cell including the access transistor to produce a difference voltage between the bitline and the complementary bitline and to apply a second plateline signal pulse to restore data to the memory cell; and

a sense amplifier circuit arranged to amplify the difference voltage.

33. (Original) A memory circuit as in claim 32, wherein the memory circuit is a ferroelectric memory circuit.

34. (Original) A memory circuit as in claim 32, wherein the first control terminal is a wordline terminal.

35. (Currently amended) A memory circuit as in claim 32, comprising:

a second control terminal coupled to receive ~~a second control signal~~ the first and second plateline signal pulses; and

a ferroelectric capacitor coupled between the access transistor and the second control terminal.

36. (Original) A memory circuit as in claim 35, wherein the second control signal produces a voltage on the bitline after the precharge signal turns off the first precharge transistor.

37. (Currently amended) A memory circuit as in claim 35, comprising:

~~a complementary bitline;~~

a second precharge transistor having a current path coupled between the complementary bitline and the voltage terminal, the second precharge transistor having a gate coupled to receive the precharge signal.

38. (Original) A memory circuit as in claim 37, comprising a third precharge transistor having a current path coupled between the bitline and the complementary bitline, the third precharge transistor having a gate coupled to receive the precharge signal.

39. (Currently amended) A method of operating a memory circuit ~~for a memory cycle~~ to reduce a charge coupled to a memory cell, comprising the steps of:

coupling the charge to the memory cell while a first control signal applied to a control terminal of the memory signal is inactive;

activating a precharge signal applied to a precharge circuit to precharge a bitline to a predetermined voltage;

activating ~~a~~ the first control signal while the precharge signal is active, the first control signal applied to ~~a~~ the control terminal of ~~a~~ the memory cell ~~transistor~~, the memory cell ~~transistor~~ having a current path connected to the bitline;

conducting at least a part of the charge to the predetermined voltage;

applying an inactive second control signal to the memory cell;

then inactivating the precharge signal; and

then activating the second control signal.

40. (Original) A method as in claim 39, comprising the step of inactivating the first control signal while the precharge signal is active.

41. (Original) A method as in claim 39, comprising the steps of:

inactivating the second control signal while the first control signal is active; and

activating the precharge signal while the first control signal is active and the second control signal is inactive.

42. (Original) A method as in claim 41, wherein the first control signal is a wordline signal, and wherein the second control signal is a plateline signal.

43. (Original) A method as in claim 42, wherein the wordline signal is applied to a first wordline and not applied to a second wordline, and wherein the plateline signal is applied to memory cells connected to the first and the second wordline.

44. (Original) A method as in claim 39, wherein the step of activating a precharge signal precharges the bitline and a complementary bitline to the predetermined voltage.

45. (Original) A method as in claim 44, wherein the predetermined voltage is Vss.